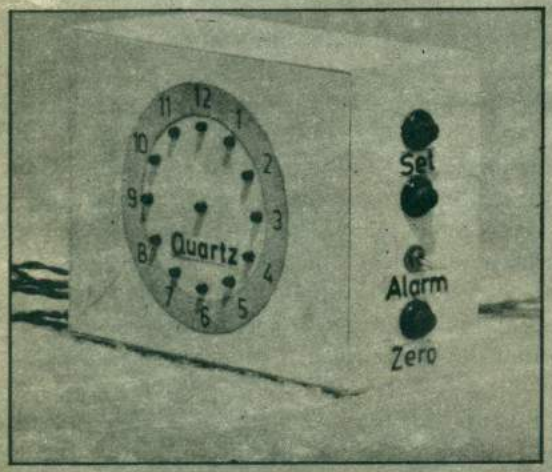
S. Batra



Pips and Alarm for LED Dial Clock

The July 1984 issue of EFY carried an LED dial clock project. Fig. 1 here shows the block schematic diagram of a modified composite LED dial clock. The middle portion shows the basic LED dial clock circuit published in the July 1984 issue. The part on its right side shows the schematic diagram of pips and alarm logic, and the part on its left-side shows the schematic diagram of a quartz controlled oscillator/divider. Both the additional circuits are presented as add-on modules. These can be assembled on a third PCB of the same (10 cm × 10 cm)

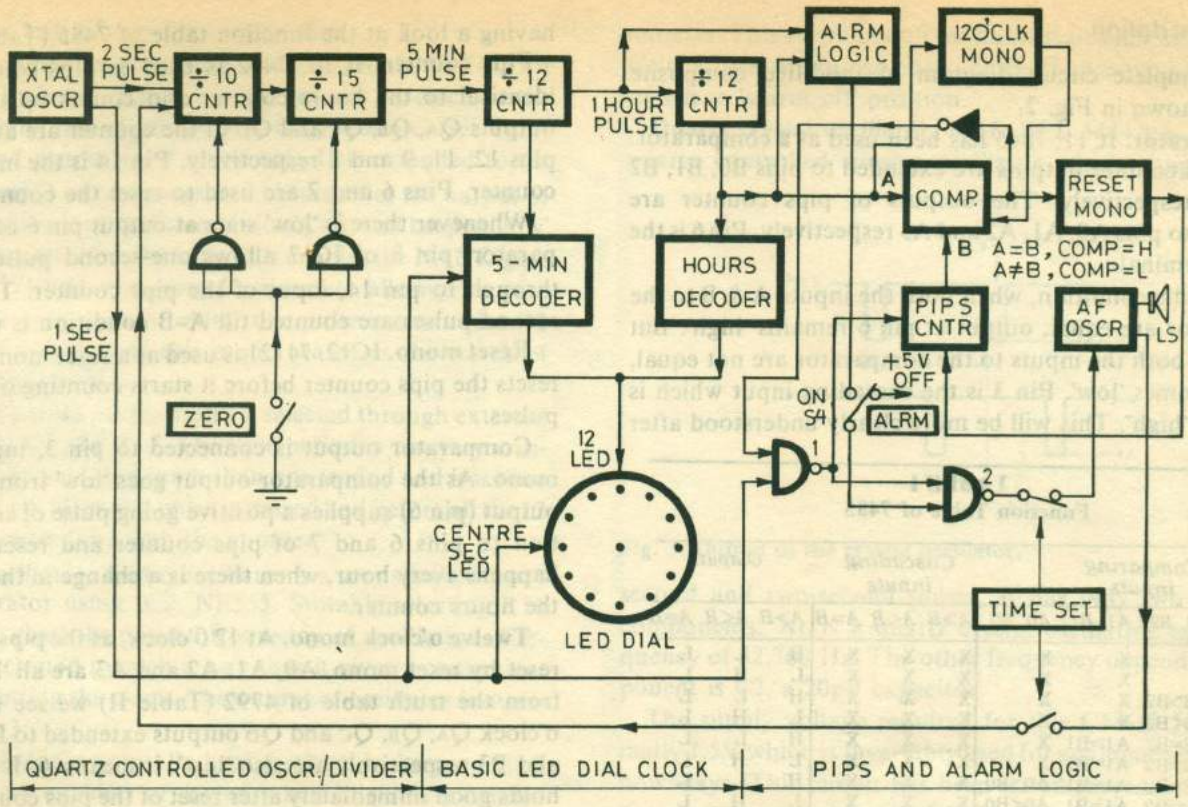


Fig. 1: Block diagram of the composite LED dial clock.

size and just added to the earlier 2-tier module of the clock to make it 3-tier, with suitable interconnections.

As you already know, the basic LED dial clock used 12 LEDs in place of 12 digits of a clock. There are neither hour/minute/second hands nor any moving part in the clock. The constantly glowing LED in its respective position in the clock-dial represents the time in hours. The minutes are represented by a blinking LED. The minute indication advances after every five minutes. The centre LED flashes every second.

Pips logic is designed on the pattern of old pendulum clocks which strike the number of hours every hour. Here the logic gives out pips through a loudspeaker every hour. Consequently, at 6 o'clock you will hear six pips and at 7 o'clock seven pips will be heard.

The alarm logic is a hard-wired fixed time logic. This logic provides continuous audio tone, say, at 6 o'clock every day. It has also been designed to produce the alarm tone for five minutes and then switch it off for the next five minutes automatically. This alarm continues for an hour unless it is switched off.

In this article the description of these additional facilities will be discussed but not of the basic LED dial clock which has already been explained in Electronic Projects Vol. 5.

Principle of working

Pips logic. The heart of this logic is a comparator. At input B of the comparator (see Fig. 1) the status from pips counter is supplied whereas at input A the status from the hours counter (ex LED dial clock) is supplied.

Whenever there is a change in the status of the hours counter, the normal A=B condition is disturbed. The comparator output resets the pips counter through a reset monostable RESET MONO and allows one-second pulses to pass through NAND gate 1 by enabling it. Enabling of gate 1 also enables gate 2 to allow audio oscillator output to pass through to the loudspeaker. The output at loudspeaker appears as pips because of one-second pulses.

Alarm logic. The alarm logic continuously monitors the status of Q_A, Q_B, Q_C and Q_D outputs of the hours counter and Q_A output of minutes counter extended from PCB1 of the basic LED dial clock. Depending upon the wiring of alarm logic and status of the said counters, alarm logic is enabled. If switch S4 is kept in alarm 'on' position, gate 2 gets 'low' from alarm logic and keys audio oscillator. This extends continuous tone of audio oscillator to the loudspeaker.

Quartz controlled oscillator/divider. Quartz controlled oscillator provides one-second and two-second pulses. Two-second pulses are divided 150 times to produce five-minute pulses. Five-minute pulses drive the basic LED dial clock. One-second pulses are extended to the centre LED and five-minute decoder.

Circuit description

The complete circuit diagram of modified composite clock is shown in Fig. 2.

Comparator. IC11, 7845 has been used as a comparator. The hours counter outputs are extended to pins B0, B1, B2 and B3 respectively. The outputs of pips counter are extended to pins A0, A1, A2 and A3 respectively. Pin 6 is the output terminal.

Under idle condition, when both the inputs A & B to the comparator are equal, output at pin 6 remains 'high'. But whenever both the inputs to the comparator are not equal, pin 6 becomes 'low'. Pin 3 is the cascading input which is normally 'high'. This will be more clearly understood after having a look at the function table of 7485 (Table 1).

TABLE I
Function Table of 7485

Comparing inputs				*Cascading inputs*			*Outputs*		
A3, B3	*A2, B2*	*A1, B1*	*A0, B0*	*A>B*	*A<B*	*A=B*	*A>B*	*A<B*	*A=B*
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	I	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Pips counter. IC10, 7492 is used as pips counter. It is identical to the hours counter and counts up to 12. The outputs Q_A, Q_B, Q_C and Q_D of the counter are available at pins 12, 11, 9 and 8 respectively. Pin 14 is the input to the counter. Pins 6 and 7 are used to reset the counter.

Whenever there is 'low' state at output pin 6 of the comparator, pin 8 of IC17 allows one-second pulses to pass through to pin 14, input of the pips counter. These one-second pulses are counted till A=B condition is obtained.

Reset mono. IC12, 74121 is used as a reset monostable. It resets the pips counter before it starts counting one-second pulses.

Comparator output is connected to pin 3, input of the mono. As the comparator output goes 'low' from 'high', Q output (pin 6) supplies a positive going pulse of small duration to pins 6 and 7 of pips counter and resets it. This happens every hour, when there is a change in the status of the hours counter.

Twelve o'clock mono. At 12 0'clock, as the pips counter is reset by reset mono, A0, A1, A2 and A3 are all 'low'. Also from the truth table of 4792 (Table II) we see that at 12 o'clock Q_A, Q_B, Q_C and Q_D outputs extended to B0, B1, B2 and B3 respectively are also 'low'. It means A=B condition holds good immediately after reset of the pips counter, with the result 'high' will be extended from the output of the comparator to NAND gate (pin 9 and 10, IC17) which inverts and disables NAND gate (pin 2, IC17). No one-second pulses get extended to the pips counter and hence no

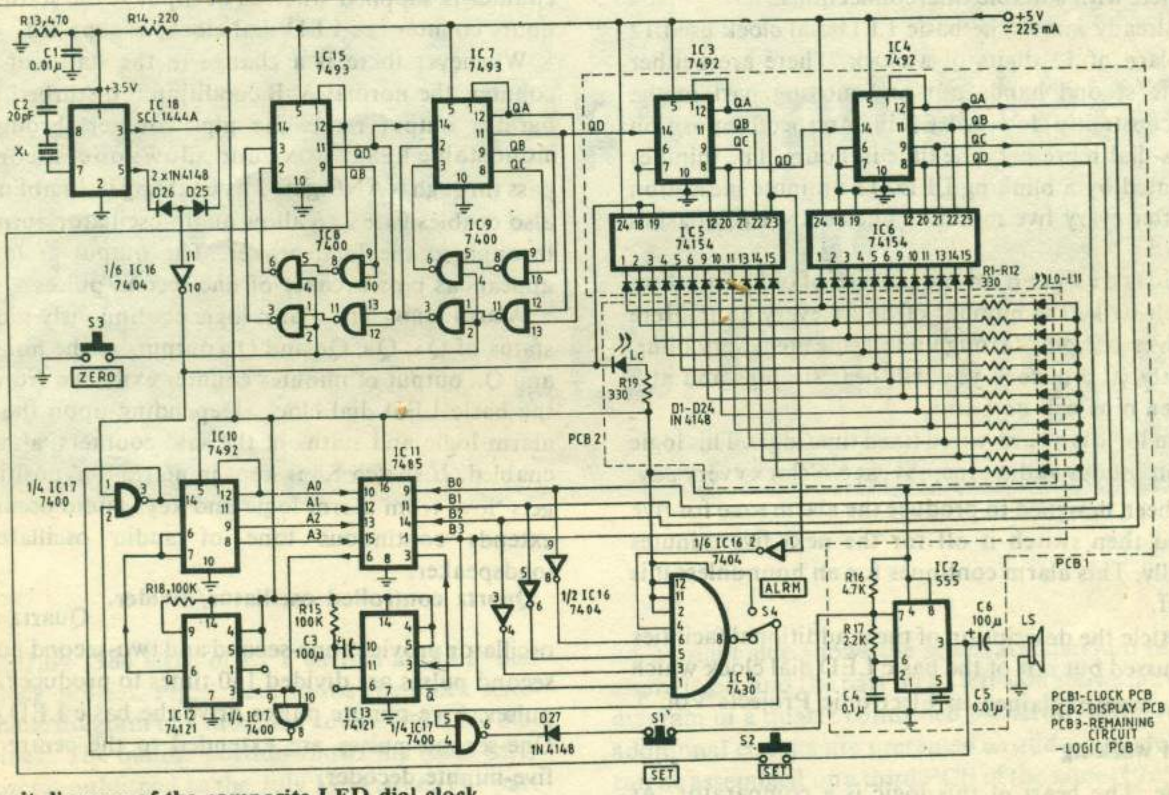


Fig. 2: Circuit diagram of the composite LED dial clock.

pips will be heard from the loudspeaker.

To overcome this problem another mono, IC13, 74121 is provided. Its input (pin 3) is triggered at 12 o'clock by the negative going transition of Q_D of hours counter (see Table II). Inverted output $\bar{Q}$ of mono (pin 1) is extended to the cascading input of comparator. This modifies the output of the comparator (under the condition A=B) and keeps it 'low' for a few seconds (see Table I). This enables the NAND gate (pin 2, IC17) and one-second pulses are allowed to pass through the pips counter. After one pulse is counted at 12 o'clock the function of this mono ceases as the status of inputs become A≠B.

The time period of this mono is selected through external components C3 and R15. The time period is not very critical. It may be anything more than one second and less than 12 seconds, i.e. after one pulse is passed and before all the 12 pulses are passed through the counter.

Audio oscillator. Audio oscillator is a very simple square wave generator using IC2, NE555. Suitably selecting R16 and R17 it gives the desired frequency of oscillation. Frequency is selected in such a way that it gives a convenient speed for setting the clock. The output of oscillator is available at pin 3.

The oscillator is normally kept disabled by keeping pin 7 'low'. It gets enabled or keyed when 'high' is extended through pin 6 of IC17.

Alarm logic. IC16, hex inverter and IC14, 8-input NAND gate form the alarm logic circuit. The input criteria is taken from Q_A, Q_B, Q_C and Q_D of hours counter and Q_A of minutes counter. The status of above criteria can be obtained from Table II at any selected time for the alarm.

TABLE II
Truth Table of 7492

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

Depending upon 0 or 1 of the above input criteria, inverter will be either included or not included in the circuit.

Fig. 2 shows the alarm logic circuit designed for 6 o'clock. When all the inputs of IC8 (pins 1, 3, 4, 5 and 6) are 'high', a 'low' from pin 8 of IC14 will allow audio tone pin 3 of IC2 to appear at loudspeaker.

From Table II we see that Q_A changes with every count. The criterion which represents count of five minutes keeps the alarm 'on' for five minutes and 'off' for the next five minutes. This continues till the hours status just changes to 7 o'clock. Alarm can also be switched off by moving the toggle switch to 'alarm off' position.

Quartz crystal oscillator. IC18, SCL 1444A is used as a quartz controlled master oscillator which supplies one-second and two-second pulses. It has only two external components. X_L is a quartz crystal oscillating at the frequency of 32,768 Hz. The other frequency dependent component is C2, a 20pF capacitor.

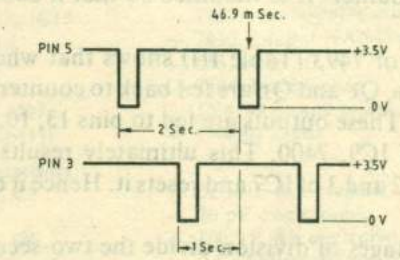


Fig. 3: Output of the crystal oscillator.

The supply voltage required for this CMOS IC is normally 1.5V which is invariably used for analogue wall clocks nowadays. This circuit has been tested successfully for an optimum supply voltage of 3.5V. This voltage is supplied through the potential divider arrangement of R13 and R14.

Two-second output is available at pins 3 and 5 separately as shown in Fig. 3. Through D25 and D26 the output is combined and extended to the gate of pips counter (pin 1 of IC17), pin 18 and 19 of minutes decoder and centre LED.

Divider IC15, 7493. The two-second output of master oscillator is fed to pin 14 of the divider. This is basically a divide-by-16 counter which was readily available instead of a decade counter.

TABLE III
Truth Table of 7493

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Having a look at the truth table of 7493 (Table III), if Q_B & Q_D is used to reset the counter it will always count up to 10

instead of 16. Therefore, the outputs of Q_B and Q_D are fed to pins 9 and 10 and pins 12 and 13 of IC 8, 7400 which in turn supply a 'high' to pins 2 and 3 of divider IC6 and reset it. Hence it counts up to 10 only.

Divider IC7, 7493. The output of divide-by-10 counter IC6 is extended to input pin 14 of IC7 which is also a divide-by-16 counter. It is modified so that it counts up to 15.

Truth table of 7493 (Table III) shows that when all the outputs Q_A, Q_B, Q_C and Q_D are fed back to counter it counts up to 15 only. These outputs are fed to pins 13, 10, 9 and 12 respectively of IC9, 7400. This ultimately results in 'high' output to pins 2 and 3 of IC7 and resets it. Hence it counts up to 15 only.

These two stages of division divide the two-second pulse by 150. In other words, a 300-second (or 5-minute) pulse is generated at the Q_D output of IC7. This is fed to basic LED

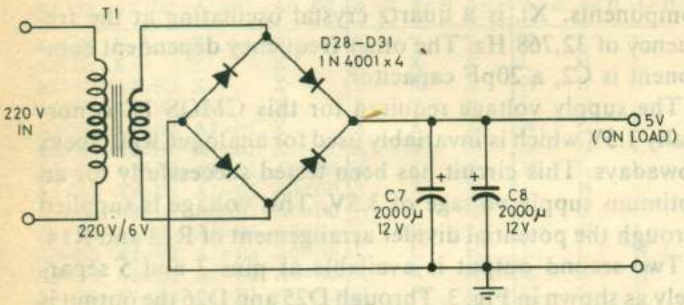


Fig. 4: Simplified power supply circuit.

dial clock pin 14 of IC3. This gives much better stability to the clock than the NE555 oscillator. That is why a quartz controlled oscillator is generally preferred.

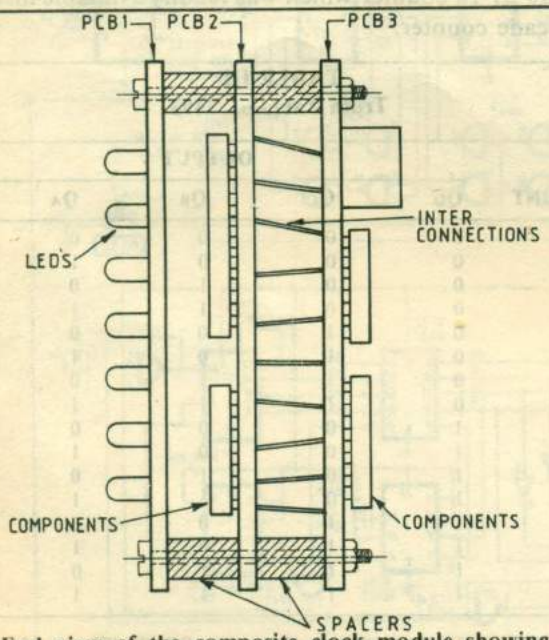


Fig. 7: End view of the composite clock module showing mounting of the third PCB.

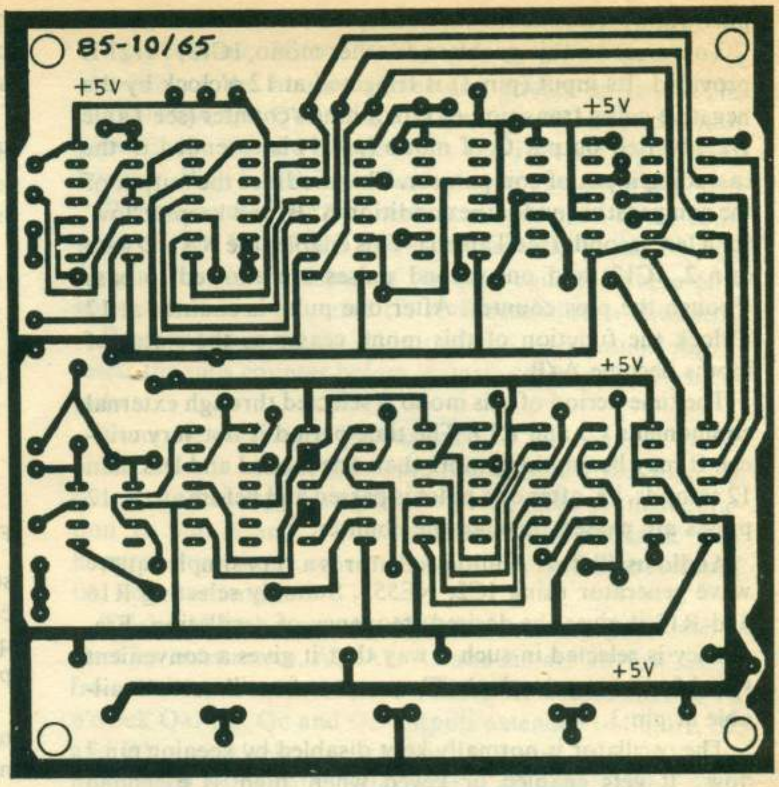


Fig. 5

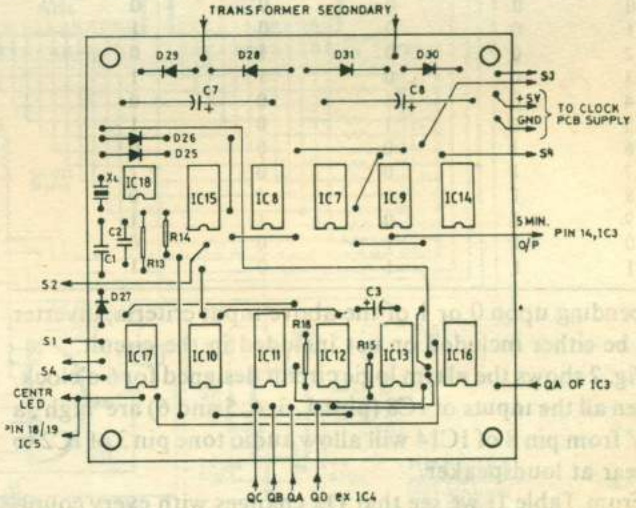


Fig. 6: Components layout of PCB 3.

Power supply

The current requirement of this circuit is about 150 mA at +5V. If the capacity of the transformer and bridge used for the power supply of LED dial clock is 500mA, the same transformer and bridge can be used to supply power to this composite clock. A simple arrangement shown in Fig. 4 will otherwise serve our purpose.

Construction

The complete circuit diagram discussed above can be assembled on a PCB of 10 cm × 10 cm, similar to the other two PCBs of basic LED dial clock. The recommended PCB layout is shown in Figs 5 and 6.

This PCB can be mounted in the third tier position, as shown in Fig. 7. The loudspeaker of 5 cm or 6.3 cm dia can be mounted on the top of the cabinet from inside with suitable fine holes drilled in the cabinet.

Controls

Setting of the clock. The clock runs fast by enabling AF oscillator. This is done by operating S4, a normally closed switch. The output of oscillator (pin 3) is extended to counter IC15 by operating switch S2. Hence by operating these two switches audio frequency is extended to the counter and the clock starts running fast so long as these switches are pressed continuously. Pressing these switches momentarily will move the clock in steps.

Zero control. After setting the clock to nearest 5-minute interval, the clock can be set precisely at any transition of 5-minute multiples. The pressing of S3, zero control, will reset the seconds counters IC6 and 7 and make the extra counted seconds to zero. If the cleared seconds counts are more than 150, operation of zero control switch will advance the 5-minute count by one besides resetting.

Alarm on/off control. This is done by a small toggle switch. One end of switch S4 is connected to 'high' permanently. This is the alarm 'OFF' condition. In the alarm 'ON' condition output of IC14, 7430 controls the enabling of NAND gate (pin 5 of IC17) which in turn keys the AF oscillator.

PART LIST

Semiconductors: (only for pips/alarm logic circuit)

IC18	— SCL 1444A, analogue clock IC
IC15, IC7	— 7493, divide-by-16 counter
IC8, IC9, IC17	— 7400, quad 2-input NAND gate
IC3, IC4, IC10	— 7492, divide-by-12 counter
IC5, IC6	— 74154, 1-of-16 line decoder
IC11	— 7485, 4-bit comparator
IC12, IC13	— 74121, monostable multivibrator
IC14	— 7430, 8-input NAND gate
IC2	— 555, timer IC
IC16	— 7404, hex inverter
D1-D27	— 1N4148 or any other diode
D28-D31	— 1N4001 diode

Capacitors:

C1, C5	— 0.01 μF disc ceramic
C2	— 20 pF disc ceramic
C3, C6	— 100 μF, 6V electrolytic
C4	— 0.1 μF disc ceramic
C7, C8	— 2000 μF, 12V electrolytic

Resistors (all ¼W, ±5% carbon):

R1-R12, R19	— 330-ohm
R13	— 470-ohm
R14	— 220-ohm
R15, R18	— 100-kilohm
R16, R17	— 4.7-kilohm

Miscellaneous:

X_L	— 32,768Hz quartz crystal
LS	— 8-ohm loudspeaker
S1	— Push-to-off switch
S2, S3	— Push-to-on switch
S4	— SPDT toggle switch
X1	— 220V to 6V, 500mA secondary transformer

Modifications

To facilitate interfacing and achieve overall improvement, the following minor modifications are required in basic LED dial clock:

(a) IC1, NE555 is discontinued which was used as 5-minute oscillator.

(b) IC2, NE555 is used as AF oscillator by changing values of its resistors.

(c) Instead of a common limiting resistor (R5) for LEDs, separate resistors are recommended to avoid small fluctuations in the constantly glowing hours LED. Hence R1 to R12 and R19 are accomodated in display PCB along with LEDs.

□